Atlas Pixel Detector Test Setup for the CPPM Production Site

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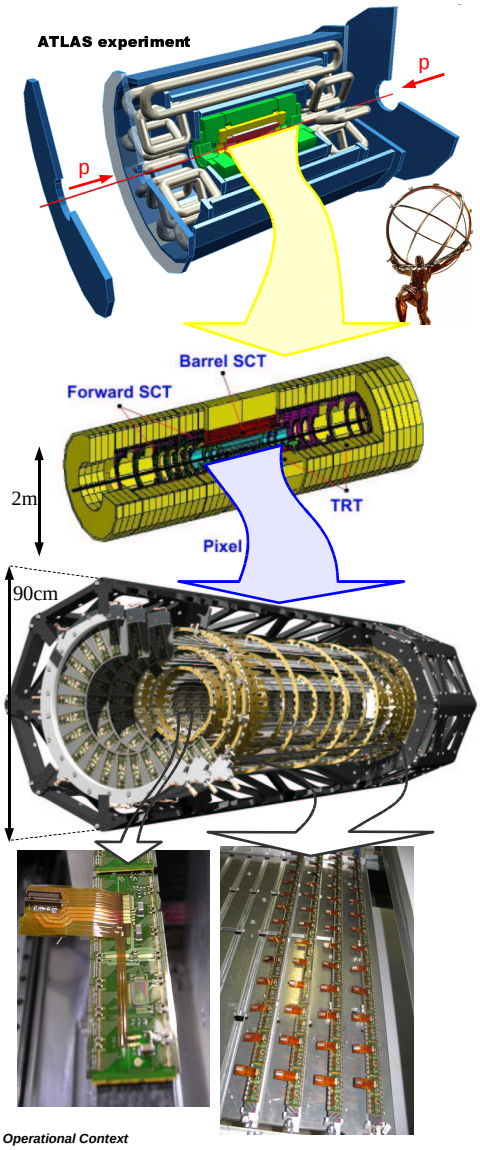
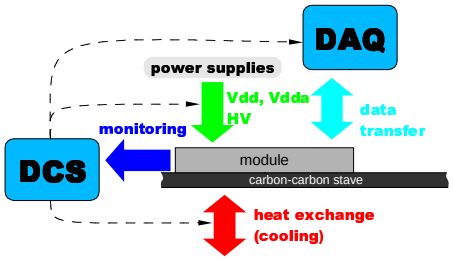
The Atlas Experiment is one of the four experiments presently being built at the Large Hadron Collider (LHC) at CERN. It comprises the Pixel Detector, a semiconductor tracking device which is traversed first by the particles emerging from proton proton collisions at the interaction point. Essential characteristics are the small size of its building blocks (16.4mm×60.8mm) and detector cells (50µm×400µm), which imply high precision during production and assembly, radition hardness and an important risk of fragility.



Operational Context

The infrastructure of a Pixel Detector module is complex. It includes three different voltages for operation. The sensitive detector areas are depleted by application of a high voltage V_{HV}, and the CMOS readout chips are supplied with two low voltages V_{dd} and V_{dda} for the digital and analog parts of the circuits. All voltages and their current consumptions as well as the module temperature measured with NTC resistors are monitored by the Slow Control System (DCS, Detector Control System). Electronic heat dissipation is principally evacuated through the carbon-carbon support, which is kept at a constant temperature of -20ºC by means of an C_3F_8 (perfluoro-propane, PFP) evaporation cooling. Data exchange with the Data Acquisition (DAQ) electronics happens digitally through serial bidirectional LVDS data lines.



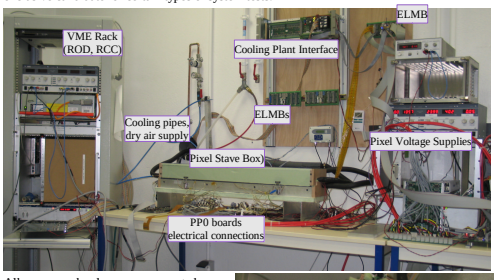
System Component Contributions

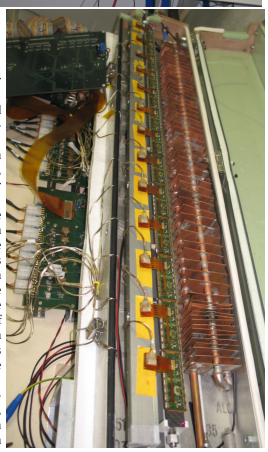
- Standalone and online Data Acquisition (DAQ) hardware [LBL]
- Data Acquisition Software [INFN Genoa, Bonn University]
- Low Voltage Regulators [INFN Milano]
- High Voltage Regulators [industrial vendor: Iseg, Germany]
- Embedded Local Monitoring Box (E-LMB) [CERN]
- PVSS environment [industrial vendor: ETM, Austria]
- PVSS software, Interlock Board and DAC plugin for ELMB [Wuppertal University]
- Completely assembled staves of the pixel detector contain contributions from Pixel Collaboration institutes in France, Germany, Italy and the USA.

System Test Concept and Setup

The production phase of the Pixel Detector has started this year and will end with the installation of the detector inside the Atlas experiment in 2006, accelerator operation being scheduled for 2007.

Our task in Marseille is to integrate, understand and use the building blocks, hardware and software, from various contributing institutes for the assembly of a **System Test Setup** which is as similar as possible to the final installation, by using the minimally required number of the original system components (or their prototypes where not available), linking and completing the system where necessary with our own ideas. This will allow us to bolster the standard production tests and complement them by long term runs in conditions in which we simulate the real environment, infrastructure and interfaces of the experiment where possible. In this way we want to identify and anticipate problems that might occur in the full scale system later. A unique feature of our setup is the prototype evaporative cooling plant, which makes it an exclusive candidate for certain types of system tests.





All necessary hardware components have been assembled in a dedicated room, where production activities have no impact on availibility or access.

Mainly two Intel-CPUs are necessary for the operation of the system:

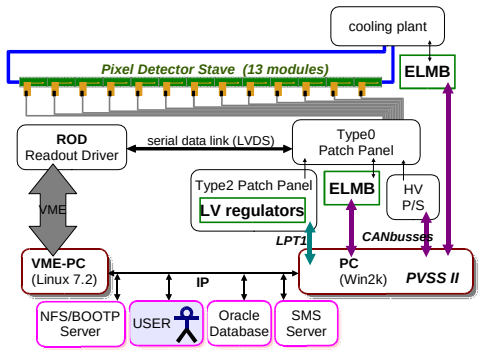
- one for detector configuration and readout functions (RCC) with VME-Interface, running under Linux RH7.2,
- and one for the slow control data acquisition within the DCS framework, running PVSS II v 3.0, under Windows 2000.

The external hardware components have been completed by an adapter board which interfaces the standard boards for voltage regulators and temperature-interlock. As this function will be implemented on detector level in the Atlas experiment, we needed to design a specific board for these small scale tests. An additional function of this board is the hardware implementation of a watchdog for the PVSS software, as the latter is crucial for safe operation of the cooling system in this context.

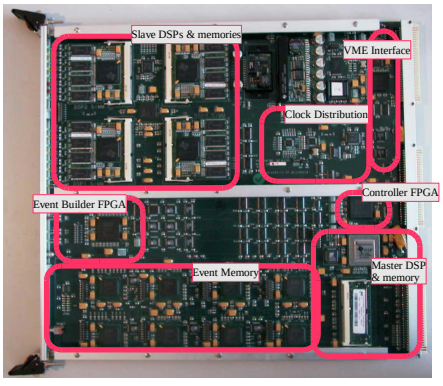
A second aspect of the small-scale implementation is a special environmental box, which provides thermal isolation and a sufficiently low dew point for safe operation of the Pixel modules (see picture above).

The control of this board and the cooling system (output) on one hand and of the slow control data acquisition (input) on the other is performed by a ATMEL128 microcontroller board (ELMB), which is Atlas wide standard and easily interfaced to PVSS.

Inter Process / Inter Component Communication (IPC/ICC) scheme



Readout Driver (ROD) board



The ROD board has various I/O functions and represents the interface between the Pixel Modules and the RCC (Readout Crate Controller) VME-PC. Three modes are essential: configuration, standalone (calibration) and online (datataking) runs. The RCC is only used in the first modes, whereas in online datataking the ROD is transparent and delivers data directly through a standard Atlas Readout Buffer (ROB) board via optical links.

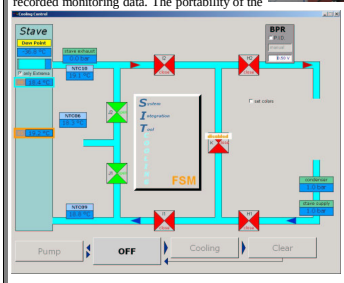
Cooling Plant

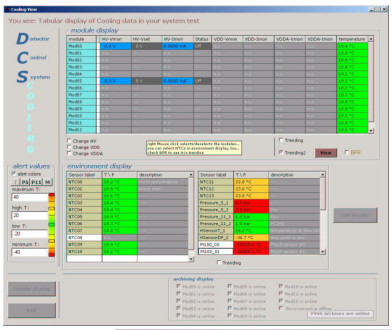
An important point in the Pixel Detector design and operation is the provision of sufficient cooling power in order to evacuate a total of 15 kW electric loss power in the whole detector (1744 modules). A 100 W evaporative cooling system with PFP (or alternatively C_6F_{10}, PFB, for higher temperature ranges) has been built in Marseille and is sufficient to evacuate the nominal 4 W of not irradiated modules right after production.

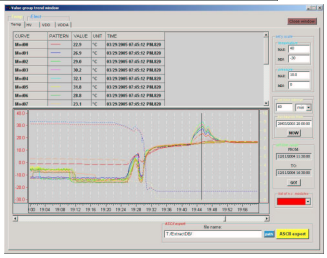
Graphical User Interfaces

The detector control (DCS) of the system is performed by the PVSS software package which will be used in the experimented and integrated in the Atlas (or even LHC) wide Experiment Control Framework.

For our specific needs we have implemented user interfaces for cooling system control as well as tools for extraction and display of recorded monitoring data. The portability of the native PVSS scripting language CTRL have been of great use and saved us some time when porting a display interface based on the *hvtracker* PVSS module developped originally for HV history display in the H1 experiment. Connection to an Oracle server, which is also part of the PVSS distribution, unfortunately turned out not to obey all specifications and obviously needs an update from the vendor in order to work correctly.







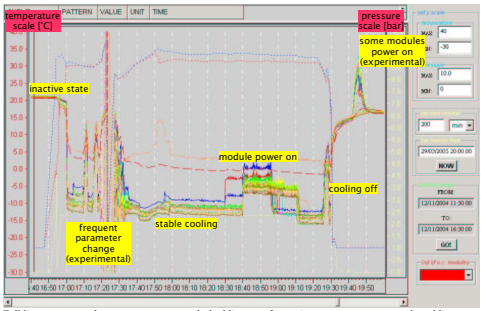
The screenshots above and on the right show :

- the control panel for the cooling plant
- the tabular view of all monitoring data in real time
- the graphical display, including the parameter options for scale and history requests to the database.

First Results

- Revelation of weaknesses of the PVSS DCS in long term operation
- Confirmationand systematic study of mechanical weaknesses of the module components (wirebonds)
- First experience with all available system components prior to integration at CERN
- Unique experience with a cooling system identical to that of the final installation
- Unique experience of simultaneous operation of 13 modules on a ROD interface

Test Run with Cooling, Low Voltage Power and Module Configuration



Full lines represent detector temperatures, dashed lines are for environment temperatures; dotted lines represent pressure measurement.

Perspectives

Tests are ongoing and many useful aspects have just been unveiled in the context of the first test runs and dedicated investigations with our testbench. The initial operation lets us expect many fruitful results and hints for improvement of the final running conditions within the Atlas experiment. Our main difficulty will be to find reasonable compromises among the priorities of the various aspects.

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