Atlas Pixel Detector Test System in Marseille

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Abstract

Prior to going into installation and operation, parts of the Atlas pixel detector are being tested outside the Atlas experiment in an environment that is as similar as possible to the final conditions, including efficient cooling at ambient temperature as well as at -20°C. A first test system has been setup and used for test run operation.

We give an overview of the hardware and software needed for a minimal setup with at least one specimen of each component and focus on local contributions, which were necessary during commissioning of our testbench.

Key words: Atlas, Pixel Detector, System Test, Slow Control, DCS, DIM, DAQ, ROD, PVSS, ELMB
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1. Atlas Pixel Detector System Test

The Atlas Experiment is one of the four experiments presently being built at the Large Hadron Collider (LHC) at CERN. It contains a Pixel Detector[1], a semiconductor tracking device which is the first to be traversed by particles emerging from proton proton collisions at the interaction point. Essential characteristics are the small size of its pixelated silicone substrates (16.4 mm$\times$60.8 mm) and detection cells (50μm$\times$400μm), which imply high precision during production and assembly, radition hardness and an important risk of fragility.

The Pixel Detector is built up from 112 staves and 6 disks, which are equipped with 1744 identical detector modules. The staves, on which concentrate the efforts reported in this article, are arranged in three concentric cylindrical barrels of 22, 38 and 52 staves. Besides a high level of irradiation in close proximity to the interaction region at LHC, critical points for operation include the evacuation of heat dissipated by the frontend electronics (approx. 1 W per module), reliable data transfer and control and stability triple voltage power supply. The assembly of the complete detector and its control, monitoring and dataking interfaces implies hardware and software contributions

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from many different production sites. In order to anticipate problems with the interplay of all components, that might occur only after final assembly, the collaboration has to set up a test system as complete as possible and in conditions that are similar if not identical to the expected reality in the final detector. Such a system should contain at least one component of all those which will be used in the final installation.

2. System Test Setup and Concept

The production phase of the Pixel Detector began in 2005 and will end with the installation of the detector within the Atlas experiment in 2006; accelerator operation being scheduled for 2007. Our task in Marseille is to integrate, understand and use the pixel modules, hardware and software, from various contributing institutes for the assembly of a system test setup which is as similar as possible to the final installation, by using the minimally required number of the original system components (or their prototypes where not available), linking and completing the system where necessary. Such a system will allow us to bolster the standard production tests and complement them by long term runs in conditions in which we simulate the real environment, infrastructure and interfaces of the experiment where possible. In this way it becomes probable to identify and anticipate problems that might occur in the full scale system later. A unique feature of our setup is the prototype evaporative cooling plant, which makes it an exclusive candidate for certain types of system tests.

In Marseille we have built the first testbench for operating a complete stave, consisting of 13 detector modules with 46,080 readout channels each, which are mounted on a thin carbon-carbon stave of approximate dimensions 2×80 cm^2. Obviously this detector is very fragile and operating temperatures above 40°C can cause severe damage to it. The nominal power dissipation of such a stave will lie around 100 W after irradiation. All necessary hardware components have been assembled in a dedicated room, where production activities have no impact on availibility or access. We have installed a complete system for automatized tests that can run for hours and later on weeks without permanent operator survey. The setup is unique being the only one equipped with an evaporative perfluoro-alcane cooling plant outside CERN. Permanent monitoring of the parameters and functional analysis of the precious detector modules, as well as the cooling system that grants a safe operating environment, requires various hardware elements, which are controlled by appropriate software. These parts of the setup correspond to those used in the final experiment and have been provided as final product samples or latest available prototypes by the institutes responsible for their production (Tab. 1). One exception from this rule is made for the optical data transfer, which is replaced by a pure electrical Back-Of-Crate (BOC) system.

Table 1
Testbench Components Contributed

• Standalone and online Data Acquisition (DAQ) hardware [LBL, Berkeley]
• Data Acquisition Software [INFN Genoa, Bonn University]
• Low Voltage Regulators [INFN Milano]
• High Voltage Regulators [2]
• Embedded Local Monitoring Box (E-LMB) [3]
• PVSS environment [4]
• PVSS software, Interlock Board and DAC plugin for ELMB [5]
Completely assembled staves of the pixel detector contain contributions from Pixel Collaboration institutes in France, Germany, Italy and the USA.

3. Cooling System

The mechanical setup, including an environmental box for dry air environment, and a small scale prototype cooling plant have been manufactured and tuned at CPPM. The provision of sufficient cooling power in order to evacuate a total of 15 kW electric loss power in the whole detector (1744 modules) is an important point in the pixel detector design and operation. A 100 W evaporative cooling system with perfluoro-propane (PFP, C_3F_8) has been built at CPPM and is sufficient to evacuate the nominal 4 W of non-irradiated modules which we are testing. The evaporation temperature at a

Fig. 1. Photography of the evaporative cooling plant used at CPPM; see fig. 5 for a schematical view. Compressor and condensor can be recognized at the lower right border. Connections to the pixel stave are positioned at the left side of the rack.

nominal pressure of 2.0 bar (abs) is $-20°$C. The cooling system has been tuned to work also with the perfluoro-butane (PFB, C_4F_{10}) in higher temperature ranges above the normal air dew point, in the range of coolant pressure from 1.5 to 3.5 bar (abs).

4. System Integration of Components

4.1. *Operational Context*

The infrastructure of a Pixel Detector module is complex (fig. 2) and includes three different voltages for operation. The sensitive detector areas are depleted by application of a high voltage HV,

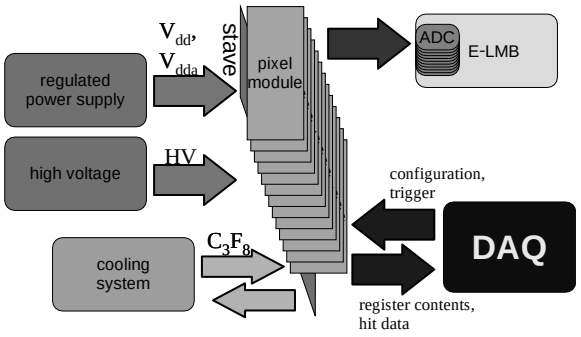

Fig. 2. Modelization of the input-output flow to and from a stave during operation: Three different voltages are needed for power supply; electric heat dissipation is lead away by evaporation of PFP (left side). Two data acquisition systems (right side) are used for slow control and datataking, where the latter is also used for detector configuration.

and the CMOS readout chips are supplied with two low voltages $V_{\rm dd}$ and $V_{\rm dda}$ for the digital and analog parts of the circuits. All voltages and their current consumptions, as well as the module temperature measured with NTC resistors, are monitored by the Slow Control System (DCS, Detector Control System). Electronic heat dissipation is principally evacuated through the carbon-carbon support, which is kept at a constant temperature of $-20°$C by means of evaporative cooling with PFP (Sec 3.). The coolant is flowing throug an aluminum cooling tube on the lower side of each stave. Data exchange with the Data Acquisition (DAQ) electronics happens digitally through serial bidirectional LVDS data lines.

Two Intel-CPUs are necessary for the operation of the system: one for detector configuration and readout functions (RCC) with a VME interface, running under Linux RH7.2, the other for the slow control data acquisition within the DCS framework, running PVSS II v 3.0, under Windows 2000.

The PVSS system reads date from LHC standard embedded local monitor boxes (E-LMB [3]) via CANbus where appropriate and possible. Other Pixel-Detector specific hardware modules, that are mainly needed for low and high voltage power supplies, are controlled via the parallel printer port (LPT2) and a proprietary

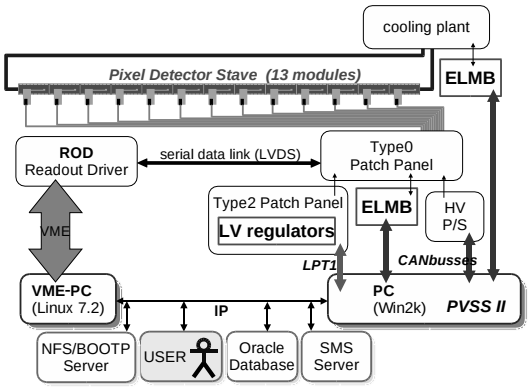

Fig. 3. Implementation of hardware connections in the Pixel Test System: The upper parts represent the frontend, whereas the lower parts stand for user interfaces and data storage. Both are connected through various hardware interface layers.

LPT1/CANbus respectively. Electronic watchdog and interlock hardware completes safety issues in case of software or network failure. The worst case scenarios to be avoided are cooling of a stave which is in an atmosphere with a dew point above atmosphere or powering a stave which is not cooled.

The external hardware components have been completed by an adapter board which interfaces the standard interlock boards (ILB) for voltage regulators and temperature-interlock. As those functions will be implemented at the detector level in the Atlas experiment, we needed to design a specific board for these small scale tests. An additional function of this board is the hardware implementation of a watchdog for the PVSS software, as the latter is crucial for safe operation of the cooling system in this context, and either software, hardware or network failures can imply loss of control and even detector damage. The control of this board and the cooling system (output) on one hand and of the slow control data acquisition (input) on the other is performed by an ATmega128L micorocontroller on ELMB boards [3], thus easily interfaced to PVSS.

A second particular aspect of the small-scale implementation is a custom environmental box, which provides thermal isolation and a suffiently low dew point for safe operation of the Pixel modules.

4.2. *Online DAQ System, ROD*

The Readout Driver (ROD) board has various I/O functions and represents the interface between the Pixel Modules and the RCC (Readout Crate Controller) VME-PC. Three modes are essential: configuration, standalone (calibration) and online (datataking) runs. The RCC is only used in the first two modes, whereas in online datataking the ROD is transparent and delivers data directly through a standard Atlas Readout Buffer (ROB) board via optical links. The function or possible degradation of the detector modules can be monitored in addition by digital or analog pulsing of the detector cells (pixels). The Readout Driver module which is used for online datataking in the final configuration contains five Digital Signal Processors (DSP), that can perform these primitive operations and also complete 2D-threshold scans autonomously and simultaneously on four detector modules in parallel. The DSPs are coordinated from a Single-Board-CPU (SBC) which controls the ROD module over VME bus. Up to 16 ROD modules will be controlled by the same SBC in the final configuration. In this sense, our testbench also serves as a testbed for the online calibration DAQ (Data Acquisition) software, that is developped in a common effort of several institutes within our collaboration.

5. Slow Control Software, DCS

The Detector Control System (DCS) is based on the commercial product PVSS [4] that has been chosen as the unique LHC-SCADA (System Control and Detector Application) across experiments and accelerator. We received the state-of-the-art development version of the AtlasPxlDCS software from the development team in Wuppertal [5], which was subsequently extended to satisfy our specific needs in Marseille. A package for automatic survey and steering of the cooling system, including a graphical user interface, valve position final state machine, display diagrams for relevant data, environment parameter watchdog and automatic operator alert has been added as explained below. Critical ranges for operating temperatures

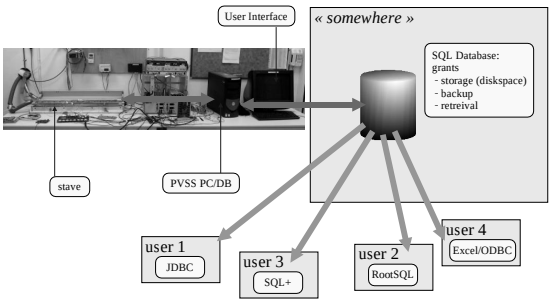

Fig. 4. Database connection design for online monitoring

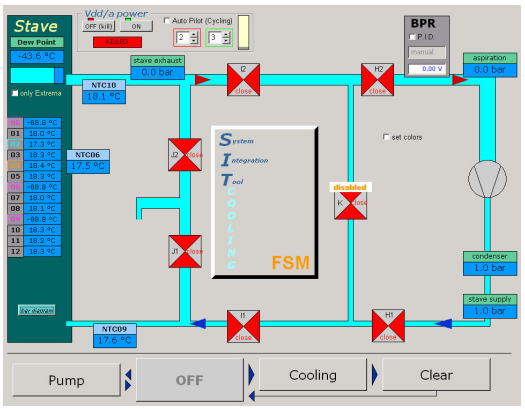

Fig. 5. Screenshot of the control panel of the cooling plant

and dew point are observed by the software autonomously and messages can be sent out via email or SMS.

5.1. *Logging to SQL Database*

Environmental values can be logged permanently in compressed format to an Oracle database instance via the ODBC/SQL interface. This opens up a large number of useful options, which are illustrated in fig. 4. Besides that, the PVSS-SQL interface enables a fast switch to other databases using SQL query standard with negligible effort and doesn't fix the choice of Oracle once and for all. This may turn out to be useful for small local database installations. On the other hand, the tools for SQL database queries support a wide range of user interfaces, including CERN standard Root [6] and commercial MS-Excel. We have used Java (JDBC) [7] and plain SQL+/PL [8].

PVSS-native connection to an Oracle server, which is also part of the PVSS distribution, unfortunately turned out not to obey all specifications and needs an update from the vendor in order to work correctly. We are using a proprietary semi-automatic version for the data transfer, which works well.

5.2. *Cooling Plant and Power Control*

The complete control and monitoring of the cooling plant has been implemented in PVSS. Electropneumatic valves are controlled via a finite state machine that prevents the user from performing illegal operations.

The same panel is also used to control the low voltages, in particular for cyclic operation (On/Off) in order to perform test programs. Powering the modules is critical and interlocked against the maximum of measured module temperatures, which makes these tests safe against cooling failures.

5.3. *DIM server for DAC-DCS interface*

The aspect of DAQ-DCS interaction and communication as well as data storage and easy extraction of relevant result data are key elements for continuous monitoring of the detector during the automatized long-term system tests. A first application runs an automatic module configuration process, whenever the power supply control software indicates an OFF-ON transition. The corresponding inter process communication is implemented in the DELPHI Information Management (DIM) [9] framework, which is now widely used in LHC and has a reliable and transparent interface to PVSS.

In conjunction with the automatic power cycling process, this server permanently surveys the status of module low voltage power. After detection of an Off-On transition, it waits for stabilization of consumption and starts configuration through the ROD board.

Fig. 6 demonstrates the encapsulation of standard and custom software elements which inter-

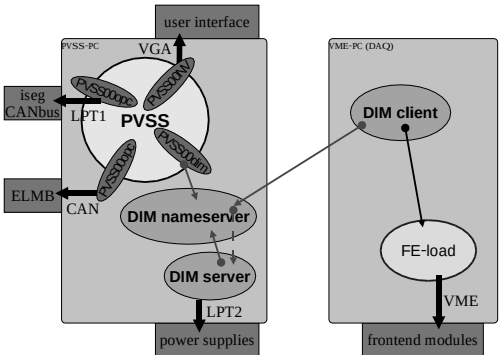

Fig. 6. Implementation scheme of inter process communication among different software elements in the system test setup

act through standard IPC software in form of the DIM package. The only new processes to implement were those of the VME-PC on the right hand side.

5.4. *Graphical User Interfaces*

We have implemented user interfaces for our specific needs in the cooling system control as well as tools for extraction and display of recorded monitoring data. The portability of the native PVSS scripting language CTRL has been of great use and saved significant time when porting a display interface based on the *hvtracker* PVSS module developed originally for HV history display in the H1 experiment [10].

Figures 7 and 8 show the graphical display, including the parameter options for scale and history requests to the PVSS database. The test run recording of fig. 7 shows steep temperature drop of 45 K in less than one minute. The temperature cycles show the typical switch-on behaviour in two steps after cooldown, the first of which results from power-on, whereas the second is the effect of increased consumption after complete configuration of all modules through the auto-configuration process (Sec. 5.3).

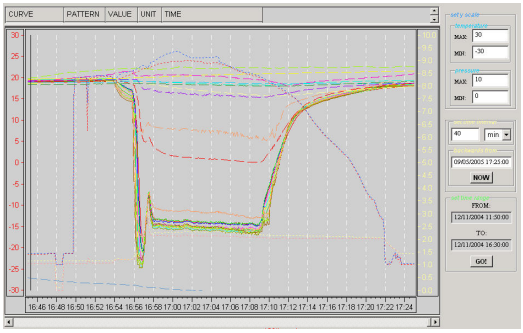

Fig. 7. Test run. Note the big temperature difference in relatively small time during cooldown

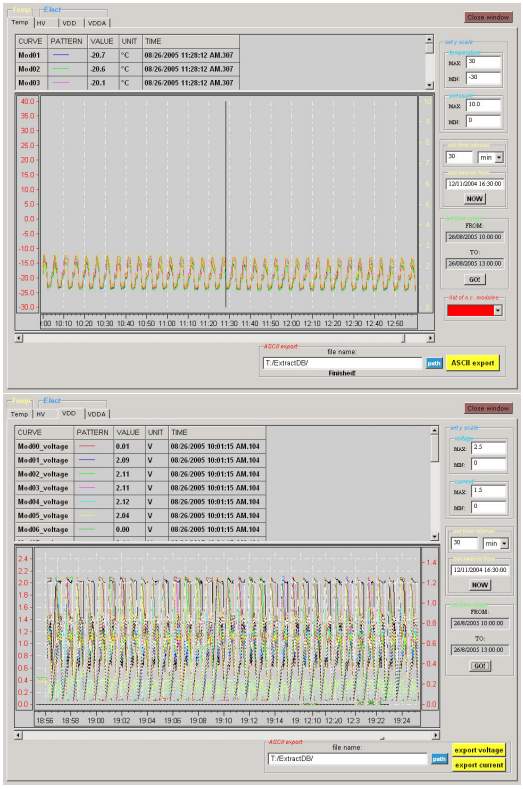

Fig. 8. Automatic temperature cycling run, seen in the temperature monitoring (top) and voltage and current monitoring panel (bottom)

6. First Results and Perspectives

Tests are ongoing and many useful aspects have just been revealed in the context of the first test runs and dedicated investigations with the testbench:

– Weaknesses of the interplay of PVSS DCS and the E-LMB hardware in long term operation have become obvious after several weeks of uninterrupted running.
– Confirmation and systematic study of mechanical weaknesses of the module components have been carried out on this testbench, for example from July to September 2005 for high gradient thermal cycling of one of the production staves in order the test the resistance of the wire bonds on the modules. More than 1000 thermal cycles have been performed and yielded a classification of the fragility of different types of wire bonds and encapsulation methods. The safety software interlocks sucessefully protected the pixel modules againt the thermal overheating during few non-standart situations.
– The first experience with all available system components prior to integration at CERN, operating a complete stave with 13 modules powered, at the only site where experiments with a cooling system identical to that of the final installation can be performed.

Extensions to the existing systems have been elaborated, that may turn out to be useful in future commissioning. The initial operation lets us expect interesting results for improvement of the final running conditions within the Atlas experiment.

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